Challenges in Empirically Testing Memory Persistency Models

V. Klimis, A. Raad, V. Vafeiadis, J. Wicker, A. F. Donaldson
Why Bother?

Ensure Hardware Vendor Accountability

Ascertain the Soundness and Strength of Persistency Semantics
Memory Persistency: The Sneaky Game of Hide and Seek

L1 cache
L2 cache
L3 cache
NVM
Litmus Test

\[
x := 1; \\
bw x; \\
\text{DSB}_{\text{full}}; \\
y := 1; \\
\text{DMB}_{\text{full}}; \\
\text{if } (a) \\
z := 1; \\
\text{rec: } (y = 1 \lor z = 1) \Rightarrow x = 1
\]

possible values of $x$, $y$, $z$ upon recovery
Persistence Domain

Intel-x86

Arm
Persistence Domain

We currently do not support building fine grained persistent memory platform solutions with the Ampere Altra SOCs. [...] That given, the Ampere Altra SOC does not have a Point of Persistence.

If the memory system does not support the Point of Persistence, a data cache clean to the PoP, DC_CVAP, behaves as a data cache clean to the PoC, DC_CVAC.
Challenges Posed by the DDR Detective

1. Virtual → Geometric Address
Challenges Posed by the DDR Detective

1. Virtual → Geometric Address

2. Address Logging, Data Omission
Challenges Posed by the DDR Detective

1. Virtual → Geometric Address

2. Address Logging, Data Omission

3. Automating DDR Detective: Lack of Command-Line Support
**Post-recovery Property:**
the possible values of x, y upon recovery
A Litmus Test

```
1: x ← posix_memalign(size ≤ L1 Cache, CACHE_LINE_SIZE)
2: y ← posix_memalign(size ≤ L2 Cache, CACHE_LINE_SIZE)
3: z ← posix_memalign(size ≤ L1 Cache, CACHE_LINE_SIZE)
4: reg ← 0
5: while time < 5 do
6:   x ← 1; dc_cwap(x); dsb(sy);
7:   y ← 1; dc_cwap(y); dsb(sy);
8:   y ← 1; dc_cwap(y); dsb(sy);
9:   z ← 1; dc_cwap(z); dsb(sy);
10:  z ← 1; dc_cwap(z); dsb(sy);
11:  z ← 1; dc_cwap(z); dsb(sy);
12: end
13: sleep(20)
14: while time < 60 do
15:   ++reg
16: // Thread 1
17: x ← reg;
18:  dc_cwap(x);
19:  dsb(sy);
20: // Thread 2
21: a ← y //thread-local register
22:  dmb(sy);
23:  if(a)
24:     z ← reg;
25:     dc_cwap(z);
26:     dsb(sy);
27: // persistency property
28: // yp = reg \lor zp = reg \Rightarrow xp = reg
29: end
```
Curiosity-driven experiments

Does DC CVAP degenerate to DC CVAC?

No sufficient statistical evidence to indicate that DC CVAP defaults to a different behaviour than DC CVAC.
Curiosity-driven experiments

Does the distance between the memory locations affect reorderings?

Larger memory chunks exhibit increased reorderings.
Curiosity-driven experiments

Do repeated persists inhibit reorderings?

As the persist repetitions grow, reorderings decrease
Curiosity-driven experiments

Does suspending the processor between writes inhibit reorderings?

Delays following persist in the litmus test decrease reorderings. The presence of a delay, rather than its specific duration, is crucial for this shift.
Curiosity-driven experiments

Does the value written make a difference?

No noticeable difference
Conclusions

- Emphasises the significance of a Tailored Validation Approach
- Showcased discrepancies between observed behaviours and vendors' specifications, underscoring the need for hands-on testing over mere reliance on documentation
- A reusable methodology to validate persistency guarantees if vendors pledge new promises in their forthcoming releases
Thanks